UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/766,944	01/30/2004	Yoshihiro Saeki	030712-24	4401

22204 7590 10/03/2005

NIXON PEABODY, LLP
401 9TH STREET, NW
SUITE 900
WASHINGTON, DC 20004-2128

EXAMINER	
WILLIAMS, ALEXANDER O	

ART UNIT	PAPER NUMBER
2826	

DATE MAILED: 10/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

H·A

Office Action Summary	Application No.	Applicant(s)	
	10/766,944	SAEKI, YOSHIHIRO	
	Examiner	Art Unit	
	Alexander O. Williams	2826	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 August 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-27* is/are pending in the application.

4a) Of the above claim(s) *5-12 and 17-25* is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1 to 4, 13 to 16, 26 and 27* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *1/30/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

Serial Number: 10/766944 Attorney's Docket #: 030712-24
Filing Date: 1/30/2004; claimed foreign priority to 10/31/2003

Applicant: Saeki

Examiner: Alexander Williams

Applicant's election of species of figures 1-3 (claims 1 to 4, 13 to 16, 26 and 27), filed 8/30/05, has been acknowledged.

This application contains claims 5 to 12 and 17 to 25 drawn to an invention non-elected without traverse.

Applicant's Pre-Amendment filed 1/20/2004 has been acknowledged.

Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

The title of the invention is not descriptive. A new title is required that is clearly indicative of the invention to which the claims are directed.

The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Claims 16, 26 and 27 are rejected under 35 U.S.C. § 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In claim 16, the use of "or" recite alternative structures. The claim language of "to be" and/or "to be further" does NOT recite positive claimed structure as a final structure of the device.

In claim 16, it is unclear and confusing to what "a fourth bonding wire electrically connecting said second bonding wire with said second electrode pad." Second electrode pad of what is connected with the second wire bonding wire?

Any of claims 16, 26 and 27 not specifically addressed above are rejected as being dependent on one or more of the claims which have been specifically objected to above.

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 to 4, 13 to 16, 26 and 27, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 102(b) as being anticipated by Brooks (U.S. Patent Application Publication # 2003/0253122 A1).

1. Brooks (figures 1 to 4) specifically figure 2 and 4 show a semiconductor chip **206** with a rectangular main surface comprising: a first side composing said main surface; a second side opposed to said first side; a main electrode pad group **(212,402)** composed of a plurality of main electrode pads, which plurality of main electrode pads is arranged on said main surface along said first side; a first electrode pad-group **(214, electrode connected to 402,212)** composed of a plurality of first electrode pads, which plurality of first electrode pads is arranged between said first side and said main electrode pad

group; a second electrode pad group **(not shown but the electrode pad connected to the end 108)** composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side; a first interconnection **213** connecting said main electrode pad with said first electrode pad; and a second interconnection **108** connecting said main electrode pad with said second electrode pad.

2. The semiconductor chip according to claim 1, Brooks show wherein said first interconnection and said second interconnection are provided on said main surface of said semiconductor chip.

3. The semiconductor chip according to claim 1, Brooks show wherein said first interconnection and said second interconnection are provided within said semiconductor chip.

4. The semiconductor chip according to claim 3, Brooks show wherein any one or both of said first interconnection and said second interconnection has or have a multi-layer wired structure.

13. The semiconductor chip according to claim 1, Brooks show wherein any one or both of said first and second interconnections is or are formed within the same wired layer.

14. The semiconductor chip according claim I, Brooks show wherein said semiconductor chip is provided with a multi-layer wired structure; and any one or both of said first and second interconnection has or have a multi-layer wired structure to which a plurality of wired layer is connected through a via in which a via hole is embedded.

15. The semiconductor chip according to claim 1, Brooks show wherein circuit elements having weak tolerance to the stress are integrated in the vicinity of the lower side of said main electrode pad group.

16. Brooks (figures 1 to 4) specifically figure 2 and 4 show a semiconductor device comprising: a substrate **202,204** having a main surface having a first range on which a first bonding pad is formed, a second range on which a second bonding pad is formed, and a third range existing between said first range and said second range; a plurality of semiconductor chips **208,206** with the same configuration to be laminated in said third range of said main surface or to be further mounted in the other semiconductor chip

laminated in said third range; each of said plural semiconductor chips with a rectangular main surface having a first side composing said main surface; a second side opposed to said first side; a main electrode pad group **212,402** composed of a plurality of main electrode pads, which plurality of main electrode pads is arranged on said main surface along said first side; a first electrode pad group **(214, electrode pads connected to 402,212)** composed of a plurality of first electrode pads, which plurality of first electrode pads is arranged between said first side and said main electrode pad group; a second electrode pad group **(not shown, but the electrode in which the 108 is connected at the end)** composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side; a first interconnection **213** connecting said main electrode pad with said first electrode pad; and a second interconnection **108** connecting said main electrode pad with said second electrode pad; a first bonding wire **220** electrically connecting said first bonding pad with said first electrode pad; a second bonding wire **222** electrically connecting said main electrode pad of said semiconductor chip with a first electrode pad of the other semiconductor chip to be mounted on said semiconductor chip; a third bonding wire **222** electrically connecting said main electrode pad of said semiconductor chip with a main electrode pad of the other semiconductor chip to be mounted on said semiconductor chip; and a fourth bonding wire electrically connecting said second bonding wire **220** with said second electrode pad; wherein, in said plural semiconductor chips, said each first side is located at the same side, each main surface is turned in the same direction, and said main electrode pad and said first electrode pad of said semiconductor chip located at the lower side are located at the outside from the first side of said other semiconductor chip located at the upper side and said plural semiconductor chips are laminated each other.

26. The semiconductor chip according to claim 16, Brooks show wherein circuit elements having weak tolerance to the stress are integrated in the vicinity of the lower side of said main electrode pad group.

27. The semiconductor chip according to claim 16, Brooks show wherein said substrate is provided with a via hole passing through from said first surface to said second surface, a via connected to said plurality of first and second bonding pads having said via hole embedded therein, and an external terminal connected to said via; and said substrate is further provided with a sealing portion sealing all bonding wires on said substrate.

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Initially, it is noted that the 35 U.S.C. § 103 rejection based on a main electrode pad group and a first electrode pad group and also a layer wired structure and a multilayer wired structure deals with an issue (i.e., the integration of multiple pieces into one piece or conversely, using multiple pieces in replacing a single piece) that has been previously decided by the courts.

In Howard v. Detroit Stove Works 150 U.S. 164 (1893), the Court held, "it involves no invention to cast in one piece an article which has formerly been cast in two pieces and put together...."

In In re Larson 144 USPQ 347 (CCPA 1965), the term "integral" did not define over a multi-piece structure secured as a single unit. More importantly, the court went further and

stated, "we are inclined to agree with the solicitor that the use of a one-piece construction instead of the [multi-piece] structure disclosed in Tuttle et al. would be merely a matter of obvious engineering choice" (bracketed material added). The court cited In re Fridolph for support.

In re Fridolph 135 USPQ 319 (CCPA 1962) deals with submitted affidavits relating to this issue. The underlying issue in In re Fridolph was related to the end result of making a multi-piece structure into a one-piece structure. Generally, favorable patentable weight was accorded if the one-piece structure yielded results not expected from the modification of the two-piece structure into a single piece structure.

Claims 1 to 4, 13 to 16, 26 and 27, **insofar as some of them can be understood**, are rejected under 35 U.S.C. § 103(a) as being unpatentable over Nakayama Sadao (Japan Publication # 2001-007278).

1. Nakayama Sadao (figures 1 to 4) specifically figure 1 show a semiconductor chip **2** with a rectangular main surface comprising: a first side composing said main surface; a second side opposed to said first side; a main electrode pad group **(second row of 13 on 2)** composed of a plurality of main electrode pads, which plurality of main electrode pads is arranged on said main surface along said first side; a first electrode pad-group **(second row of 13 on 2)** composed of a plurality of first electrode pads, which plurality of first electrode pads is arranged between said first side and said main electrode pad group; a second electrode pad group **(third row of 12 on 2)** composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side; a first interconnection connecting **13** said main electrode pad with said first electrode pad; and a second interconnection **14** connecting said main electrode pad with said second electrode pad.

2. The semiconductor chip according to claim 1, Nakayama Sadao show wherein said first interconnection and said second interconnection are provided. on said main surface of said semiconductor chip.

3. The semiconductor chip according to claim 1, Nakayama Sadao show wherein said first interconnection and said second interconnection are provided within said semiconductor chip.

4. The semiconductor chip according to claim 3, Nakayama Sadao show wherein any one or both of said first interconnection and said second interconnection has or have a multi-layer wired structure.

13. The semiconductor chip according to claim 1, wherein any one or both of said first and second interconnections is or are formed within the same wired layer.

14. The semiconductor chip according claim I, Nakayama Sadao show wherein said semiconductor chip is provided with a multi-layer wired structure; and any one or both of said first and second interconnection has or have a multi-layer wired structure to which a plurality of wired layer is connected through a via in which a via hole is embedded.

15. The semiconductor chip according to claim 1, Nakayama Sadao show wherein circuit elements having weak tolerance to the stress are integrated in the vicinity of the lower side of said main electrode pad group.

16. Nakayama Sadao (figures 1 to 4) specifically figure 1 show a semiconductor device comprising: a substrate **1** having a main surface having a first range on which a first bonding pad **5** is formed, a second range on which a second bonding pad **5** is formed, and a third range existing between said first range and said second range; a plurality of semiconductor chips **2,3** with the same configuration to be laminated in said third range of said main surface or to be further mounted in the other semiconductor chip laminated in said third range; each of said plural semiconductor chips with a rectangular main surface having a first side composing said main surface; a second side opposed to said first side; a main electrode pad group **(second row of 13 on 2)** composed of a plurality of main electrode pads, which plurality of main electrode pads is arranged on said main surface along said first side; a first electrode pad group **(second row of 13 on 2)** composed of a plurality of first electrode pads, which plurality of first electrode pads is arranged between said first side and said main electrode pad group; a second electrode pad group **12** composed of a plurality of second electrode pads, which plurality of second electrode pads is arranged on said main surface along said second side; a first

interconnection connecting **13** said main electrode pad with said first electrode pad; and a second interconnection **14** connecting said main electrode pad with said second electrode pad; a first bonding wire **11** electrically connecting said first bonding pad with said first electrode pad; a second bonding wire **10** electrically connecting said main electrode pad of said semiconductor chip with a first electrode pad **4** of the other semiconductor chip to be mounted on said semiconductor chip; a third bonding wire **10** electrically connecting said main electrode pad of said semiconductor chip with a main electrode pad of the other semiconductor chip **3** to be mounted on said semiconductor chip; and a fourth bonding wire electrically connecting said second bonding wire with said second electrode pad; wherein, in said plural semiconductor chips, said each first side is located at the same side, each main surface is turned in the same direction, and said main electrode pad and said first electrode pad of said semiconductor chip located at the lower side are located at the outside from the first side of said other semiconductor chip located at the upper side and said plural semiconductor chips are laminated each other.

26. The semiconductor chip according to claim 16, Nakayama Sadao show wherein circuit elements having weak tolerance to the stress are integrated in the vicinity of the lower side of said main electrode pad group.

27. The semiconductor chip according to claim 16, Nakayama Sadao show wherein said substrate is provided with a via hole passing through from said first surface to said second surface, a via connected to said plurality of first and second bonding pads having said via hole embedded therein, and an external terminal connected to said via; and said substrate is further provided with a sealing portion sealing all bonding wires on said substrate.

Therefore, it would have been obvious to one of ordinary skill in the art to use the main electrode pad group and the first electrode pad group and a layer wired structure and a multilayer wired structure as "merely a matter of obvious engineering choice" as set forth in the above case law.

The listed references are cited as of interest to this application, but not applied at this time.

Field of Search	Date
U.S. Class and subclass: 257/777,686,685,723,784,786,676,202,203,207,208,210,211,698,690,691,692,693	9/28/05
Other Documentation: foreign patents and literature in 257/777,686,685,723,784,786,676,202,203,207,208,210,211,698,690,691,692,693	9/28/05
Electronic data base(s): U.S. Patents EAST	9/28/05

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Alexander O. Williams whose telephone number is (571) 272 1924. The examiner can normally be reached on M-F 6:30AM-7:00PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Nathan Flynn can be reached on (571) 272 1915. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Alexander O Williams
Primary Examiner
Art Unit 2826

AOW
9/28/05